Amendments to Specification

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a schematic buck diagram of a buck converter according to the present invention;

Figure 2 shows the waveforms of the operating signals of the circuit of Figure 1;

Figure 3 is a schematic block diagram of a circuit to determine how soon the converter goes into discontinuous mode;

Figure 4 shows the waveforms of the operating signals of the circuit of Figure 3;

Figure 5 is a schematic block diagram of a circuit that will block operation of the present invention due to a glitch in the TRIP signal;

Figure 6 shows the waveforms of the operating signals of the circuit of Figure 5;

Figure 7 is a schematic block diagram of the feedback block 112 of Figure 1;

Figures 8a and 8b are graphs of theoretical converter characteristics showing the designers control over the output voltage of the present invention and the prior art;

Figure 9 is a circuit implementation of the schematic block diagram of Figure 3;

Figure 10 is a circuit implementation of the schematic block diagram of Figure 5;

Figures 11A – 11D [is] are a circuit implementation of the schematic block diagram of Figure 7;

Figure 12 illustrates a simulated response of the circuits shown in Figures 9-11D; and

Figure 13 is a schematic block diagram of a boost converter in accordance with the present invention.